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RESEARCH ARTICLE

Examination and experimental comparison of dc/dc buck converter topologies used in wireless electric vehicle charging applications

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ABSTRACT

The studies on Wireless Power Transfer (WPT) technology and peripherals in Electric Vehicle (EV) applications are intensifying. While the energy received from the WPT system is transferred to the EV battery, the direct current (dc)/dc converter circuits are used. The dc/dc buck converter topologies are one of them. The converter circuits must be highly efficient, lightweight, and compact to have a high range in EV vehicles. There are asynchronous buck, synchronous buck, and interleaved synchronous buck converter circuit topologies from the literature. In this study, the efficiency results of these circuit topologies were analyzed using MATLAB/Simulink and experimental studies. This study contributes to the literature by conducting circuit-level efficiency analysis and component-level power loss analysis. It has been observed that the interleaved synchronous buck converter circuit operates at 99% efficiency at 1066 W. In addition, it has been shared with the oscilloscope results that the current ripples of this circuit topology are lower than other circuit converters. Specifically, there has been a significant reduction of 56% in power losses, particularly in the interleaved synchronous buck converter (ISBC). This study analyzes the dynamic behavior of the dc/dc buck converter topologies, and results about their performance are given.

1. Introduction

Electric vehicles play a crucial role in sustainable transportation solutions, standing out prominently as an eco-friendly alternative to fossil fuel-dependent conventional vehicles [1]. The growing demand requires developing and optimizing charging infrastructure for electric vehicles [2]. In this context, wireless charging systems for electric vehicles represent a significant technological advancement with the potential to make the charging process more user-friendly, accessible, and practical to reach a higher user rate. The wireless power transfer (WPT) system [3, 4] enables the transfer of energy by utilizing primary and secondary coils used for charging electric vehicles [5]. Figure 1 illustrates an example of a WPT system. This system includes two main parts: the ground station and the electric vehicle side.

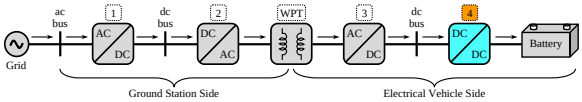

Figure 1. Unidirectional wireless power transfer system

On the ground station side, high-frequency alternating current (ac) is obtained to feed the coils on the primary coil of the WPT system. Firstly, ac obtained from the grid is rectified to direct current (dc) using an ac/dc converter. The obtained dc energy is then converted back to high-frequency ac energy using a dc/ac converter, making the primary coil ready for energy transfer. The electrical vehicle side includes the secondary side of the WPT system and has a battery connection. Different circuit structures and control algorithms play an important role during energy flow from the secondary coil to the battery. Some control techniques include primary control [6] and secondary side control [7]. This study implements secondary side control, where the ac energy at the output of the secondary coil is transferred to the battery using an ac/dc full bridge diode rectifier and a dc/dc converter in the block 4 (dc/dc) in Figure 1. The battery current and voltage are controlled by this converter, allowing for a more precise management of the charging process.

When examining battery charging systems [8], different dc/dc topologies [9] come into play. Buck converters are employed in applications with lower

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battery voltage than the dc bus voltage. The dc bus is located between block 3 (ac/dc) and block 4 (dc/dc) in Figure 1.

Within the scope of buck converters, dc/dc buck converter topologies such as asynchronous buck, synchronous buck, and interleaved synchronous buck [10] will be comprehensively discussed. The asynchronous buck topology is a commonly used switching power converter type in dc/dc converters. The synchronous buck, unlike the asynchronous buck, incorporates a semiconductor switch. This reduces losses occurring on the diode, potentially increasing circuit efficiency and optimizing dynamic performance. The interleaved synchronous buck [11] topology is achieved by parallel operating multiple synchronous buck converters. This can provide higher efficiency and lower current ripples in high-power applications. This article will thoroughly discuss the performance of these topologies in battery charging applications.

This study includes the following sections: Section II asynchronous buck, synchronous buck, and interleaved synchronous buck converter circuit topologies and control algorithms are explained. Section III includes MATLAB/Simulink simulation studies of these dc/dc buck converters. Section IV describes the experimental study stages and gives the dc/dc buck converters' current, voltage, and efficiency comparisons. Section V covers the conclusion section.

2. dc/dc buck converter topologies

In power electronics converter applications, the dc/dc buck converter circuits reduce dc output voltage [12]. In this study, asynchronous buck converter (ABC), synchronous buck converter (SBC), and interleaved synchronous buck converter (ISBC) topologies were examined. The total circuit efficiency decreases when high powers are reached in the conventional asynchronous buck converter circuit [13]. In dc/dc buck converter circuit topologies, ISBC topology transfers power at high efficiency [14].The following headings explain the ABC, SBC, and ISBC topologies.

2.1. Asynchronous buck converter (ABC)

The ABC topology has the conventional dc/dc buck circuit structure. In this circuit topology, there is a switch and a diode. Depending on the control algorithm, the S1 is switched at a determined duty cycle rate. When S_1 is closed, current flows through the switch and inductance towards the output in Figure 2 (a). In this case, D_1 is closed, and no current flows through the diode. When the S_1 is open, D_1 turns into conduction due to inductance counter-electromotive force (CEMF) in Figure 2 (b).

The ABC circuit's continuous conduction mode (CCM) operating states are detailed in Figure 2.

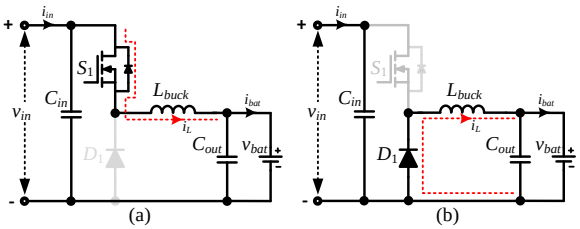


Figure 2. Operation modes of the asynchronous buck converter: (a) S_1 is on, (b) S_1 is off

Asynchronous buck converter output voltage depends on the v_{bat_ABC} duty cycle D ratio and can be written as in Eq. (1).

$$v_{bat\_ABC}=v_{in}\,D \tag{1}$$

where; v_{in} is the input voltage of the ABC. The inductance L_{buck} and capacitor C_{out} values in the ABC circuit can be determined by Eq. (2) and Eq. (3), respectively.

$$L_{buck}=\frac{v_{in}\,(v_{in}-v_{bat})}{f_s\,\Delta i_L\,v_{in}} \tag{2}$$

$$C_{out}=\frac{\Delta i_{L\_ABC}}{8\,f_s\,\Delta v_{bat}} \tag{3}$$

where; f_s is the switching frequency, Δi_{L_ABC} is the inductor ripple current, Δv_{bat_ABC} is the output voltage ripple. In this study, i_{L_ABC} is designed to be a maximum of 20%, v_{bat_ABC} is designed to be a maximum of 0.15%, and these values are expressed as:

$$\Delta i_{L\_ABC}=\frac{D\,(v_{in}-v_{bat})}{f_s\,L_{buck}} \tag{4}$$

$$\Delta v_{bat\_ABC}=\frac{\Delta i_{L\_ABC}}{8\,f_s\,C_{out}} \tag{5}$$

When the S_1 is closed, the inductance operates at v_{in}–v_{bat} voltage. When S_1 is open, it induces a CEMF equal to the inductance voltage v_{bat}. The following equation can express inductance voltage according to the S_1 position.

$$\begin{cases} v_{in}-v_{bat}=L_{buck}\dfrac{di_{L\_ABC}}{dt} & |\ S_1\text{-}on \\ -v_{bat}=L_{buck}\dfrac{di_{L\_ABC}}{dt} & |\ S_1\text{-}off \end{cases} \tag{6}$$

2.2. Synchronous buck converter (SBC)

The difference between the synchronous buck converter circuit and the asynchronous topology [15] is that there is an S_2 instead of a D_1. The voltage drop on D_1 in the ABC circuit is higher than on a semiconductor switch. This situation causes high losses in high-power applications. The SBC topology is preferred in high-power applications due to low voltage drop and less power loss. The SBC circuit structure and current flow diagram according to operating states are given in detail in Figure 3. In the SBC circuit, S_1 and S_2 are operated with a phase shift of 180°.

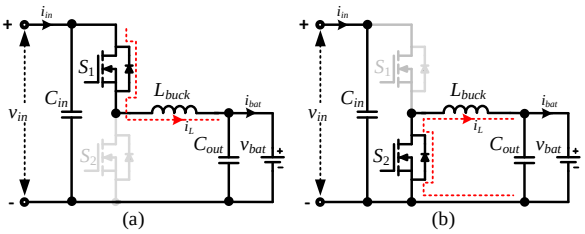


Figure 3. Operation modes of the synchronous buck converter: (a) S_1 is on, S_2 is off, (b) S_1 is off, and S_2 is on

The voltage gain of the SBC circuit can be described by Eq. (1) in the CCM as in the ABC structure. Because the only difference between the ABC and SBC is the use of SIC MOSFET instead of a diode, the output current and output voltage ripple of the SBC circuit can be calculated by Eq. (4) and Eq. (5), respectively, as in the ABC topology.

2.3. Interleaved synchronous buck converter (ISBC)

In conventional dc/dc buck converter circuits, inductance losses increase when high currents are reached. The interleaved topology structure shares the total current transferred to the output $i_L=i_{L1}+i_{L2}$. In this topology structure, more than one phase arm is created, and an inductance is connected to each. Thus, the losses of switching elements and the volumes of passive circuit elements can be reduced. The ISBC [16] circuit topology and operating ranges used in this study are detailed in Figure 4. The S_1-S_4 and S_2-S_3 switches in the ISBC circuit are switched with a phase shift of 180°.

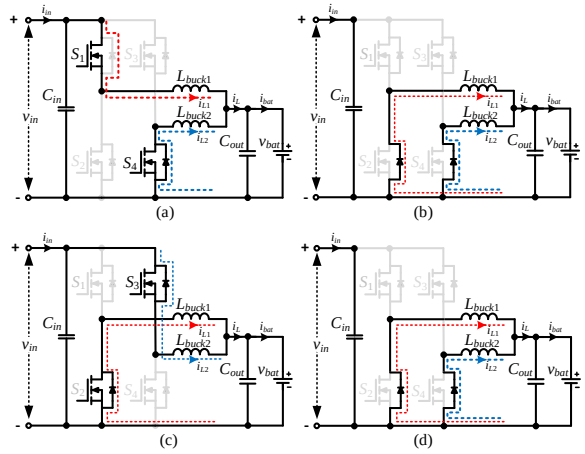


Figure 4. Operation modes of the interleaved synchronous buck converter: (a) S_1 and S_4 are on, S_2 and S_3 are off, (b) S_1 and S_4 are off, and S_2 and S_3 are on

In the ISBC circuit, the output current equals the sum of the coil currents. In this converter structure, when D 0.5, the output current ripple is theoretically equal to 0. The voltage gain of the ISBC circuit can be described by Eq. (1) in the case of the CCM as in the ABC structure. The output current ripple of the ISBC circuit can be explained as follows.

$$\Delta i_{L\_ISBC}=\frac{v_{bat}\,D\,(1\text{-}2D)}{L_{buck1}\,f_s} \tag{7}$$

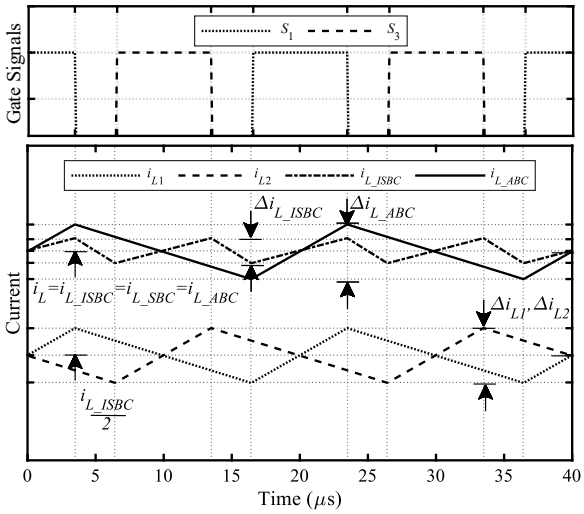


Figure 5. Gate signals and idealized current waveforms of the SBC and ISBC circuits

Since the two inductances in the ISBC structure reduce the current ripple, the voltage fluctuations at the circuit output are half as much as in the ABC circuit topology and are expressed as in Eq. (8).

$$\Delta v_{bat\_ISBC}=\frac{\Delta i_{L\_ISBC}}{16 f_s\,C_{out}} \tag{8}$$

Figure 5 shows the inductance and the output current waveforms depending on the gate signals of the SBC and the ISBC circuits. In the idealized current waveforms, the output current ripple of the ISBC circuit is lower than the SBC circuit.

Advantages of the ISBC circuit topology: reduced input and output capacitors, high efficiency at high load currents, improved thermal performance, and low voltage ripple during load transitions [16]. Table 1 gives the design parameters of the dc/dc buck converter circuits used in this study.

Table 1. System the design parameters of the dc/dc buck converter topologies

Descriptions	Parameters	Value
Input dc bus voltage	v_{in}	200 V
Maximum input dc current	i_{in_max}	17 A
Maximum battery voltage	v_{bat_max}	200 V
Maximum battery current	i_{bat_max}	25 A
Nominal power	P_{nom}	3.5 kW
Inductance	L_{buck}	500 μH
Inductance resistance	R_{Lbuck}	40 mΩ
Input capacitance	C_{in}	560 μF × 2 || 4 470 nF || 4
Input capacitance resistance	R_{Cin}	54 mΩ (560 μF) 4.49 mΩ (470 nF)
Output capacitance	C_{out}	560 μF 470 nF
Output capacitance resistance	R_{Cout}	54 mΩ (560 μF) 4.49 mΩ (470 nF)
Inductance current ripple	Δi_L	20 %
Capacitance voltage ripple	Δv_C	0.15 %
Voltage PI$_1$ block	$Kp_1 - Ki_1$	0.2 – 0.05
Current PI$_2$ block	$Kp_2 - Ki_2$	0.01 – 1e-6

2.4. Control algorithms of the dc/dc buck converter topologies

This study used a battery group representing the electric vehicle (EV) battery. The EV battery group was charged with a closed-loop control method using the constant voltage method. Reference voltage values were entered into the control algorithm for three different situations: 160 V, 185 V, and 195 V, depending on the battery's state of charge (SOC).

Current reference is produced by the PI_1 block according to the measured voltage and defined reference voltage value of the EV battery group. Then, the PI_2 block has a switching signal according to the battery current and reference current value. The EV battery group's maximum charging current is i_{bat_ref} 25 A. Figure 6 shows the block diagram of the closed-loop control algorithm of the dc/dc buck converters. In the study, the ABC, SBC, and ISBC circuit switches at 50 kHz with a triangular carrier and comparator. The dead time between switches in the same branch is 200 nS. Table 1 gives the PI block coefficients in the control algorithm. The saturation limits for the PI_2 outputs are set with a minimum of D_{min} 0 and a maximum of D_{max} 1.

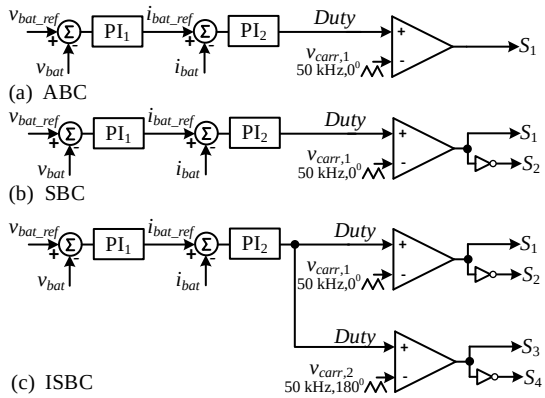


Figure 6. Block diagram of the control algorithm of the dc/dc buck converter topologies: (a) for the ABC, (b) for the SBC, and (c) for the ISBC

2.5. Operation area analysis

This study used a lithium iron phosphate ($LifePO_4$) battery with a capacity of 9.6 kWh was used as the EV battery group. The operating voltage of the battery group varies between 160 V – 200 V, and the charge graph at 1C is given in Figure 7.

This study determined the dc bus voltage at the dc/dc buck converter input as 200 V. Different voltages are needed to charge the EV battery group. For this reason, a dc/dc buck converter was used in the wireless EV charging system. When the charging graph of the EV battery group is examined, there is a voltage demand of 160 V and 200 V.

In this study, the EV battery group was charged with constant voltages of 160 V, 185 V, and 195 V, respectively.

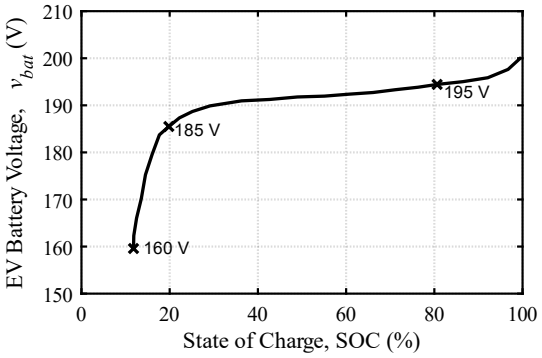


Figure 7. Charging graph of the $LiFePO_4$ type EV battery rated 9.6 kWh capacity

The battery charging and discharging operations are performed to keep the SOC within the range 20% to 80% for health of the battery. Therefore, 185V and 195V voltage values are selected. Additionally, the circuit's performance at the minimum voltage is examined, while the maximum voltage of 200V is excluded. Because D 1 is required to achieve 200V output voltage. For this D value, the SIC MOSFET always on, and the diode remains in an always off. In this configuration, SIC MOSFET has only conduction losses without any switching losses, as diode has no losses. Thus, the system's performance is analyzed where the D is less than 1. Initially, it was charged with 160 V until the SOC reached 20% to avoid charging at a high current for battery health. Then, the EV battery group was charged with a high current at 185 V until the SOC reached 80%. Finally, the battery charging process was completed with 195 V and a low current. This means there are different operating areas for different current and voltage levels. In this study, the performances of the dc/dc buck converter topologies in different operating areas were examined in detail.

3. Experimental and simulation results

A modular power circuit was prepared for the ABC, SBC, and ISBC circuits in the study. The experimental setup includes all power stages, measurements, and control units that enable the EV wireless charging. The experimental setup photo is given in Figure 8. The dc/dc buck converter part in the whole circuit given in the Figure 9 was examined for this study. The dc/dc buck converter part in the total circuit was examined for this study. The control unit contains an STM32H750 microcontroller of the STMicroelectronics. Wolfspeed brand's C3M0045065K model SIC MOSFET with 650 V, 49 A, and 4.5 mΩ internal resistance was used as the semiconductor switch in the power circuit. SIC MOSFETs are switched with Infineon Technologies' 1ED020I12B2XUMA1 model gate driver integrated circuits. Differential PWM's are applied to input of gate driver. Differential PWM signals may exhibit greater resilience against potential electromagnetic interference. In this study, the PWM signals is converted into a differential form by using a ST26C31BDR model differential line driver. Wolfspeed brand's E3D20065D SIC diode with 650 V

and 56 A rated was preferred for the reverse diode in the ABC circuit. The filter capacitors contain 560 µF aluminum electrolytic and 470 nF film capacitors of the Wurth brand. The inductances were produced as 52 turns using Magnetics brand 0078617A7 number ferrite core toroid material and 4mm^2 wire. AMC 1301 integrated circuit is used as a voltage sensor and LEM CAS 25-np is used as a current sensor. These sensors provide data to the microcontroller. A signal conditioning circuit is necessary to connect these sensors to the microcontroller. This circuit both converts the sensor output data to a suitable voltage level for the microcontroller and additionally protects the microcontroller ADC inputs. Chroma 62000S-H 600 V 17 A programmable power supply was used at the dc input of the dc/dc buck converter circuits. Auxiliary power supply (UTP3315TFL-II) was used to provide 12V for circuits such as control card, gate driver, fans, etc. Voltage probe (Pintek DP25) and current probe (TCPA3000) were used to measure input and output voltage and current data. These probes are compatible with both oscilloscope and data acq card (NI USB 6356). While the oscilloscope shows the signals waveform on its screen, daq card can transfer the measured data to computer.

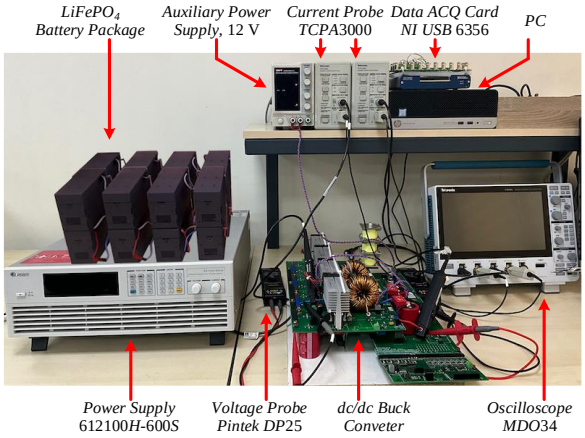


Figure 8. Photograph of the experimental setup

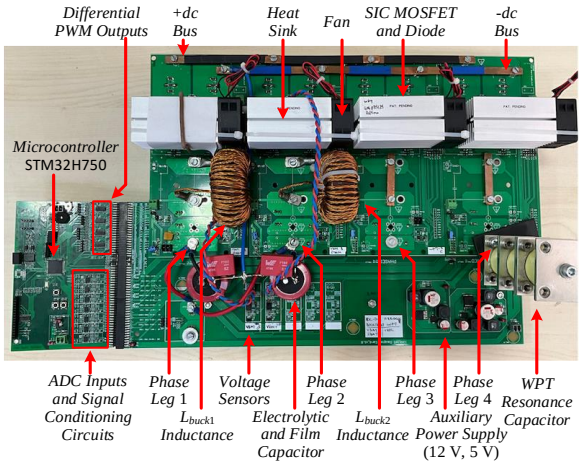


Figure 9. Photograph of the dc/dc buck converter and the control board

The 200 V 24 Ah rated LifePO$_4$ EV battery was connected to the output of the dc/dc buck converter circuits. Since the input/output current and voltage graphs of the ABC and SBC circuits are the same, the oscilloscope results for the SBC topology are given in Figure 10. In this operating state, the input voltage and current of the SBC circuit are 198.7 V and 7.856 A, and the output voltage and current are 149.2 V and 10.58 A. In this case, the EV battery group is charged with 1578 W. The oscilloscope results also give the gate signals of the SIC MOSFETs in the circuit.

The ISBC circuit was operated at the same input/output voltage and current values as the SBC circuit. In this case, the input/output current and voltage graphs of the ISBC circuit are given in Figure 11. In this case, the total circuit output current is the same as the SBC and 10.79 A. However, it is understood from the oscilloscope that the total current is shared with the two inductances in the circuit $i_L=i_{L1}+i_{L2}$. The current ripples in SBC and ISBC circuits are Δi_{L_SBC} 1600 mA and Δi_{L_ISBC} 840 mA, respectively. Experimental results have shown that the current ripple at the ISBC circuit output decreases.

In the experimental study, a comprehensive investigation of circuit-level efficiency and component-level power loss was conducted. The efficiency measurement at the circuit level, which constitutes the first phase, was examined for ABC, SBC, and ISBC.

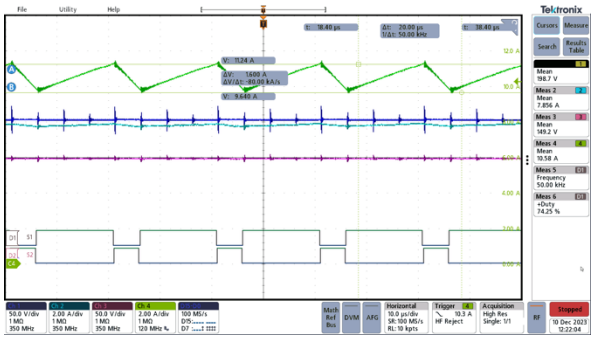


Figure 10. The input/output voltage and current waveforms of the SBC circuit (Ch$_1$:v_{in}, Ch$_2$: i_{in}, Ch$_3$: v_{bat}, Ch$_4$: i_L)

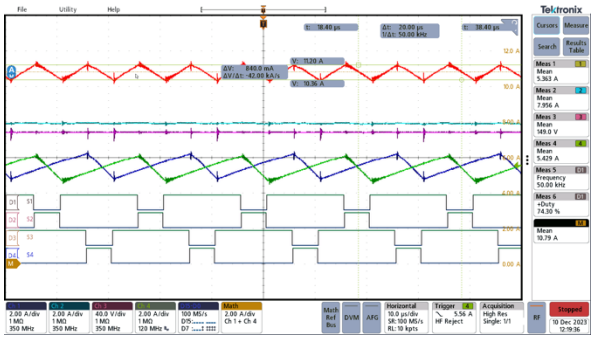


Figure 11. The input/output voltage and current waveforms of the ISBC circuit (Ch$_1$: i_{L_buck2}, Ch$_2$: i_{in}, Ch$_3$: v_{bat}, Ch$_4$: i_{L_buck1}, Ch$_{math}$: $i_{L\_buck1}+i_{L\_buck2}$)

In the second stage, a component-level loss analysis was performed to explore the factors affecting efficiency during transitions between circuit

topologies, specifically focusing on the losses associated with the diode, SIC MOSFET, and output capacitor. The first component-level analysis aims to explain the shift from ABC to SBC by conducting a loss analysis for the diode and SIC MOSFET on the low side. Another loss analysis was carried out for the transition from SBC to ISBC to help explain the reasons behind the high-side SIC MOSFET losses. The final component-level study involves power loss analysis on the output capacitor.

Firstly, for circuit-level efficiency analysis of the dc/dc buck converter, the topologies mentioned in the study were modeled with MATLAB/Simulink. The simulation processes considered the circuit elements' internal resistances and conduction losses. The dc/dc buck converter circuits were run in a simulation environment at three different charging voltages. The dc-to-dc efficiencies were analyzed in simulation studies depending on the dc/dc buck circuit output powers. The comparison graph of the obtained simulation and experimental results is given in Figure 12. According to this power-efficiency graph, it can be seen that the modeling and experimental results coincide. When simulation results are compared to experimental results, the letter shows higher values. This difference between them is derived from factors including parasitic elements, simulation model accuracy, measurement errors, nonlinear behavior of components, etc.

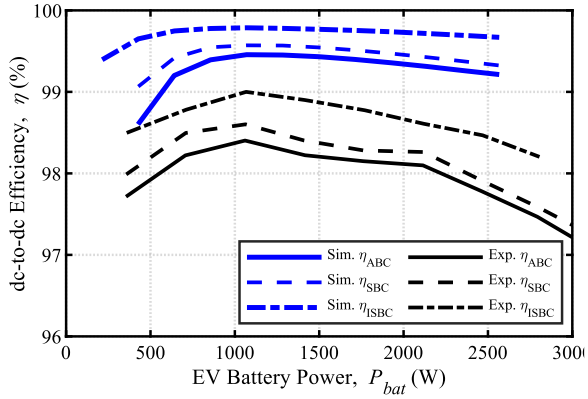


Figure 12. Simulation and experimental efficiency graph for v_{bat} 185 V according to the output power change of the dc/dc buck converters

According to experimental results, Figure 13 shows the efficiency contour graphs on the voltage/current axes of dc/dc buck converter topologies. In these efficiency graphs, the maximum efficiencies of the ABC, SBC, and ISBC circuits are 98.3%, 98.5%, and 99%, respectively. In the literature, some studies provide 97% [17], 95% [18], 93% [19], and 92% [20] efficiency for ISBC. Compared with the studies in the literature, satisfactory results were achieved thanks to the SIC MOSFET and two-phase structure of dc/dc converter.

At high current values, higher values of the ISBC circuit efficiency have a wider operating area. The simulation and experimental studies conducted in this study show that the ISBC circuit, one of the dc/dc buck converter topologies, should be preferred in the charging circuits of EVs due to its high efficiency.

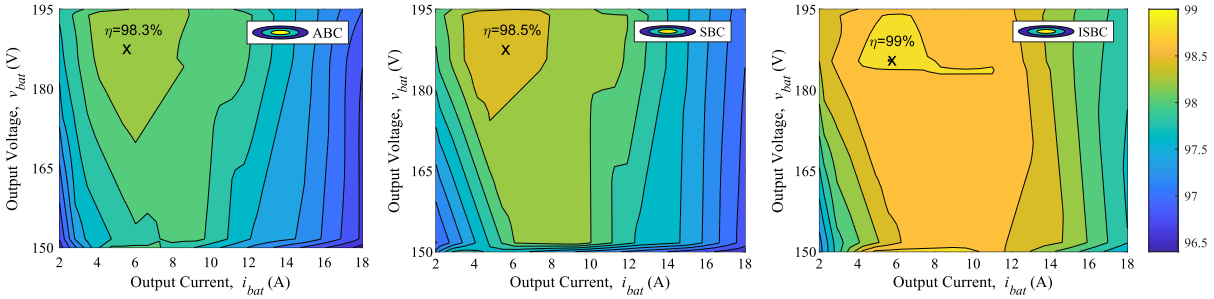
The diode, SIC MOSFET, and output capacitor were selected due to their lifecycle considerations in the component-level loss analysis. The voltage stress and current stress on the component result in power losses. The power loss brings about a thermal swing on the component. This thermal swing contributes to a reduction in the component's lifespan. Therefore, in the component-level analysis, graphs depicting instantaneous power variations on the component are provided to better understand and address these issues.

The first component-level analysis aims to explain the shift from ABC to SBC by conducting a loss analysis for the diode and SIC MOSFET in the low side. The SBC circuit uses a SIC MOSFET (S_2) instead of the diode (D_1) used in the ABC circuit. The total loss occurring on the diode and SIC MOSFET is composed of conduction and switching losses. Figure 14 illustrates these power losses. The instantaneous power on the graph represents the loss occurring on the diode for the ABC, while it indicates the loss on the SIC MOSFET for the SBC. The diode losses in the ABC are mitigated in SBC by employing MOSFETs instead of diodes. The power loss graph was obtained using the currents and voltages across D_1 and S_2. The figure shows that the instantaneous power loss on the ABC diode is greater than the instantaneous power loss on the SIC MOSFET.

When the average values are calculated, $P_{D1\text{-}ABC}$ 39.72 W and $P_{S2\text{-}SBC}$ 34.17 W Calculating the loss ratio with reference to diode losses, the loss of the S_2 switch is 14% lower, resulting in an 86% loss

A second component-level loss analysis was carried out for the change from SBC to ISBC to help explain the reasons behind the high-side SIC MOSFET losses. Figure 15 illustrates S_1 SIC MOSFETs of the SBC and ISBC switching losses. The power loss graph was obtained using the currents and voltages across the elements S_1 SIC MOSFET of the SBC and ISBC. As illustrated in Figure 15, the instantaneous variations in the total loss predominantly arise from the conduction losses during the conduction phase of the SIC MOSFET. The figure shows that the instantaneous power loss on the S_1 SIC MOSFET of the SBC is greater than the instantaneous power loss on the S_1 SIC MOSFET of the ISBC. When the average values are calculated, $P_{S1\text{-}SBC}$ 10.31 W and $P_{S1\text{-}ISBC}$ 4.56 W Calculating the loss ratio with reference to the SBC, the loss of the ISBC is 56 % lower, resulting in an 44% loss.

The final component-level study involves power loss analysis on the output capacitor. Figure 16 illustrates the instantaneous power on the output capacitor of the SBC and ISBC. This graph is plotted using the voltage across the capacitor and the current flowing through it. The maximum current value on the capacitor is 0.5 A for the SBC, whereas it is 1.0 A for the ISBC.



(a) (b) (c)

Figure 13. Contour efficiency graphs of the dc/dc buck topologies according to the experimental study's different current and voltage values: (a) for the ABC, (b) for the SBC, and (c) for the ISBC

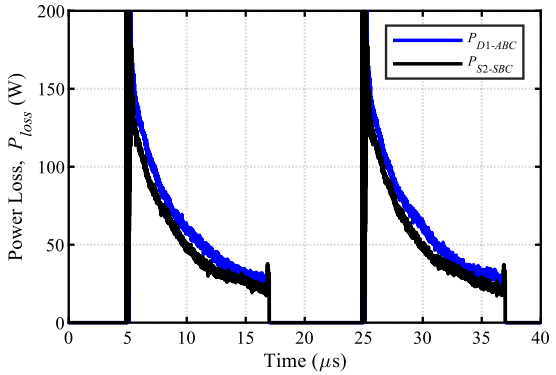


Figure 14. D_1 diode of the ABC and S_2 SIC MOSFET of the SBC instantaneous power for D=0.4 and P_{bat}=1050W according to the experimental of the dc/dc buck converters

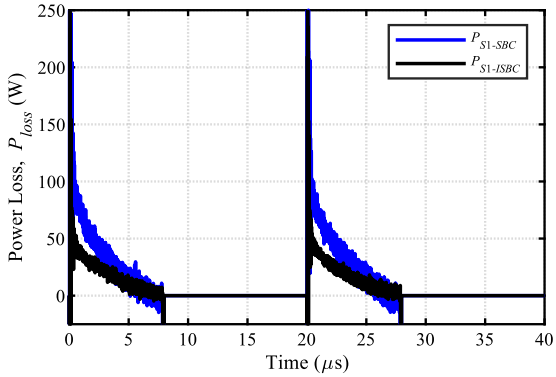


Figure 15. S_1 SIC MOSFET of the SBC and ISBC instantaneous power for D=0.4 and P_{bat}=1050W according to the experimental of the dc/dc buck converters

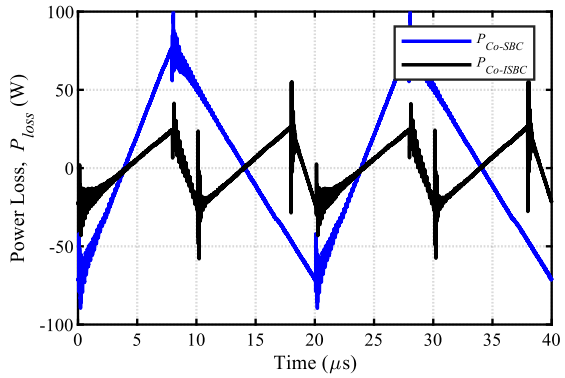


Figure 16. Output capacitor of the SBC and ISBC instantaneous power for D=0.4 and P_{bat}=1050W according to the experimental of the dc/dc buck converters

Consequently, the power loss due to the internal resistance of the output capacitor is reduced in the ISBC. The given equivalent series resistance value R_{Cout} in the table is 54 mΩ. A small loss is expected considering the capacitor current and this R_{Cout} value. When the average values are calculated, $P_{Co\text{-}SBC}$ 17.8 mW and $P_{Co\text{-}ISBC}$ 10.8 mW Calculating the loss ratio concerning SBC, the loss of the ISBC is 40% lower, resulting in a 60% loss.

4. Conclusion

This study analyzed the simulation and experimental results of the dc/dc buck converter topologies used in electric vehicle wireless charging systems. The fact that this converter circuit inside the vehicle in EVs is light, low-volume, and high-efficiency will increase the vehicle's range. This study shares the results of asynchronous buck, synchronous buck, and interleaved synchronous buck converter circuit topologies in the literature. In experimental test results, the ABC circuit was operated with 98.3% efficiency at 1060 W power, the SBC circuit with 98.5% efficiency at 1063 W power, and the ISBC circuit with 99% efficiency at 1066 W power. The loss analysis has revealed that the most significant losses occur across the diode between SIC MOSFET and the output capacitor. This emphasizes the advantage of change from ABC to SBC. Moreover, the loss analysis indicates that transitioning to the ISBC from SBC results in a more advantageous circuit, as the current phases are shared, enhancing the overall efficiency of the circuit. These circuit-level and component-level results show that the ISBC circuit topology should be preferred as it operates with low current ripple and high efficiency at high powers. Compared with the studies in the literature, satisfactory results were achieved thanks to the SIC MOSFET and the ISBC structure of the dc/dc converter.

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